ELKTRONICS
VIDEO DISPLAY GENERATOR VDG-1

The unit is designed to work to the 525 line NTSC standard, and as such is not suitable for use outside the USA.

The Elektronics VDG-1 Video ID board is a self contained module that will produce a quick source of computer video upon applying power. Four computer generated graphics screens are stored in a 27C128 E-PROM, two high-resolution screens and two colour bar patterns are available. These screens are located within different areas of the E-PROM's memory and are selected by controlling several address lines by means of four single-pole/double-throw switches wired to positions SW1 to SW4 on the printed circuit board. The output from the unit is standard 525 line NTSC at a level of 1 volt peak-to-peak, which can be connected direct to your ATV transmitter input, video monitor or video recorder. There is also a video relay in the circuit which routes live video through when the power is turned off. To identify your transmission, or for use as a test pattern, just turn on the ID board and the relay will switch from the through video to the generated picture. Finally, an automatic sequencer/timer featured in the circuit allows you to sequence through all four screens, or several combinations of two screens, varying from 0.2 seconds per screen up to a maximum of one minute per screen.

CIRCUIT DESCRIPTION

The circuit diagram of the unit is shown in Fig.1 The clock frequency to drive the 6847 Video Display Generator (VDG) IC is derived from a 3.579545MHz crystal, using part of the MC1327P IC as an oscillator. The VDG then generates all of the signals necessary to produce a video waveform. The computer graphics information stored in the 27C128 E-PROM is accessed by the VDG to produce the desired graphics screen. In combination with the control signals from the VDG the MC1372P functions as a colour/video mixer which adds in the colour burst signal. The composite waveform is then fed to a two transistor video amplifier to produce the final output signal.

The four graphics screens contained in the E-PROM are designed using a Radio Shack colour computer and then down-loaded into the memory device. The two high-resolution screens occupy approximately 6144 bytes of memory each, and the two colour bar patterns 512 bytes each. A memory map for the E-PROM is shown in Fig.2. High res. screen 1 and colour bar 1 are located in the lower 8k of the device, whilst the other two screens are held in the upper 8k. To switch between the lower and upper areas of memory address line A13 is raised high by means of switch SW3, or by the timer/sequencer section of the circuit dependant on the position of SW4.

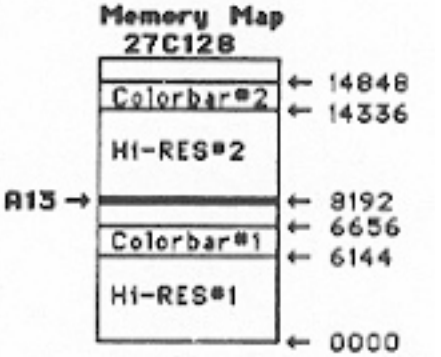

Fig.2 E-PROM Memory Map

To select the colour bar patterns the CD4066 analog switch IC is switched by the settings of SW1 and SW2, and used to disconnect the E-PROM address lines A11 and A12 from VDG control, connecting them to logic high. The VDG is also switched to the graphics mode.

The VDG device is only designed to produce a black and white picture in the high-resolution mode. To overcome this a 555 Timer IC is used to generate the correct timing pulses for the MC1327P to allow a colour signal to be generated. While producing a colour video output this method does have two anomalies. Firstly, if the output is viewed on an oscilloscope it can be seen that the colour burst extends throughout the horizontal sync pulse. However, this has no effect on the video quality. The second problem is due to the fact that the VDG may start on either the rising or the falling edge of the clock pulse, thus there is a chance of getting reversed colours on the high res screens (ie: blues will be red and vice-versa). To correct this simply turn off the power supply and turn on again, repeating if necessary until the correct colours are observed. These problems only occur with the high resolution screens, correct colours are always generated in the low resolution mode used for the colour bars.

The video output waveforms of the board are shown in Fig.3. The 'white' level generated by the VDG is actually a light shade of grey, thus a ratio of 0.40 volts of sync pulse to 0.62 volts of video should be measured as shown.

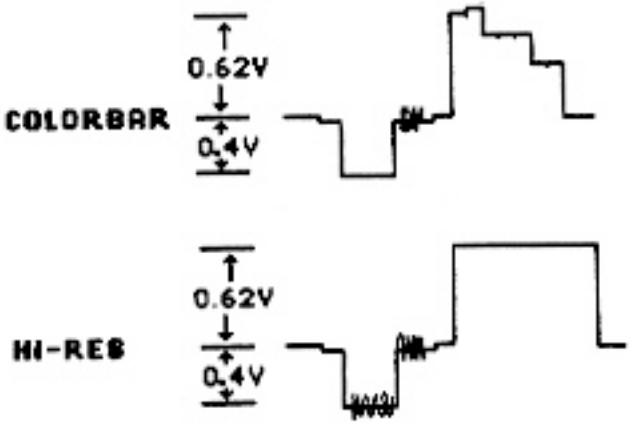

Fig.3 Video Output Waveforms

The sequencer/timer function is controlled by a 2240 Timer IC. This chip is used to generate two timed outputs to control the selection of the VDG high res/colour bar mode, and the switching of the E-PROM memory banks.

The timing of the display and its sequences are selected by the four switches SW1 to SW4. Table-1 gives the various permutations of the switches and the displays obtained. The board as supplied has links fitted at SW1 and SW4 to provide automatic sequencing through all four screens. These links must be removed before installing the switches. The switches should be wired as shown in Fig.4 so that the centre pin of the switch is connected to the centre pad of the switch PCB location. Position each switch so that when in the up position the top two pads on the PCB for that switch location are connected together, this is the ON position as referred to in table-1.

Switches SW1 and SW4 control the timer functions, SW2 and SW3 control the manual selection of the screens when SW1 and SW4 are both in the off position.

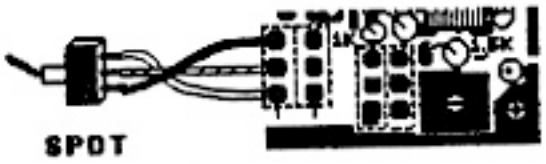

Fig.4 Switch Wiring

SW1	SW2	SW3	SW4	SCREENS SELECTED
ON	X	X	X	Sequences through all four screens.
OFF	ON	X	ON	Sequences through the two high-res screens.
OFF	OFF	X	ON	Sequences through the two colour bar screens.
ON	X	ON	OFF	Sequences through high-res 2 and colour bar 2.
ON	X	OFF	OFF	Sequences through high-res 1 and colour bar 1.
OFF	ON	ON	OFF	Manually selects high-res screen 2.
OFF	ON	OFF	OFF	Manually selects high-res screen 1.
OFF	OFF	ON	OFF	Manually selects colour bar screen 2.
OFF	OFF	OFF	OFF	Manually selects colour bar screen 1.

X = Position does not matter.

Table 1. Screen select combinations.

NOTE: For repeater applications where computer control of the graphics screens selection is desired links should be fitted between the bottom two pads of SW1 and SW4. Apply a TTL level signal (+5v) from the repeater control circuit to the centre pads of SW2 and SW3 to control the screen selection.

SETTING UP

The locations of the various connection points and potentiometers is shown on the PCB overlay in Fig,5.

All that is required to be done is to wire up unit, the switches and other remote controls and the inputs and outputs.
A suitable enclosure is the TEN-TEC JW-5 or the Hammond 1590C.
The video input and output connectors should ideally be the BNC variety. The power supply for the unit should be connected via 1nF feed-through capacitors to reduce RF interference.

Connect a monitor or oscilloscope to the output and switch the unit on. Set the VIDEO GAIN potentiometer to the 10 o'clock position and adjust the SYNC LEVEL potentiometer until a video output is present. Set up the switch positions as per table-1 to output one of the colour bar patterns. Re-adjust the SYNC LEVEL potentiometer until the yellow colour bar begins to 'white out'. The SYNC LEVEL control should be backed off until the point is reached where the yellow bar restores to normal colour. The VIDEO GAIN control is now adjusted to give the desired output level. This level may need optimising to give a correct balance between the generated screens and any through video being connected to the VIDEO INPUT, this being passed to the transmitter when the ID board is powered-down. Please note that adjustment of the VIDEO GAIN control beyond the halfway position may result in sync compression.

If external control of the timing circuit is required remove the 500k TIMER ADJUST potentiometer from the printed circuit board and install a chassis mounted type on the front panel. If longer delay times than one minute are required this potentiometer may be increased in value.

This completes the set-up procedure and the unit may now be connected into your ATV transmit system. The screens available are only limited by your imagination and Bill's (or your) computing talents.

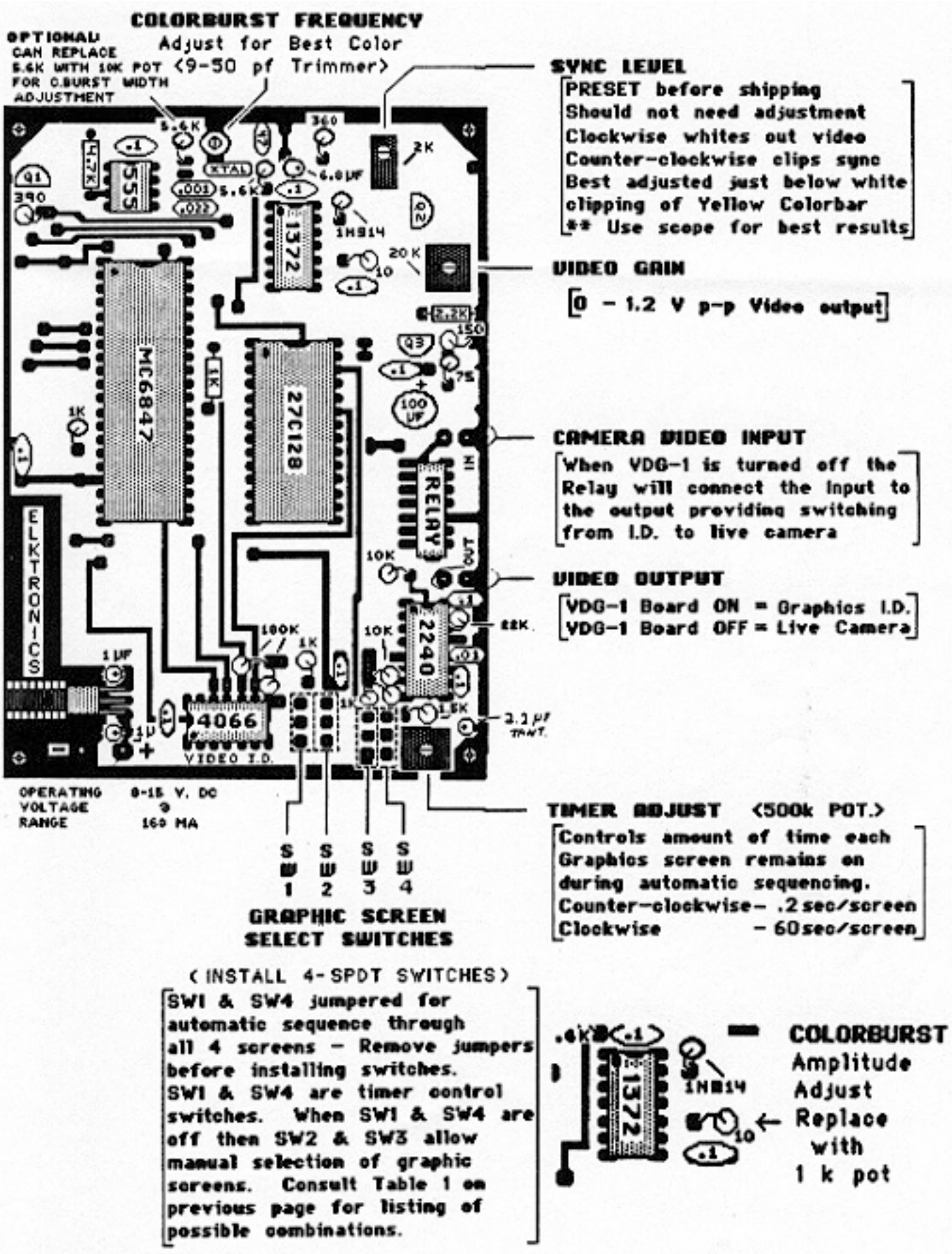

Fig.5 Component Layout

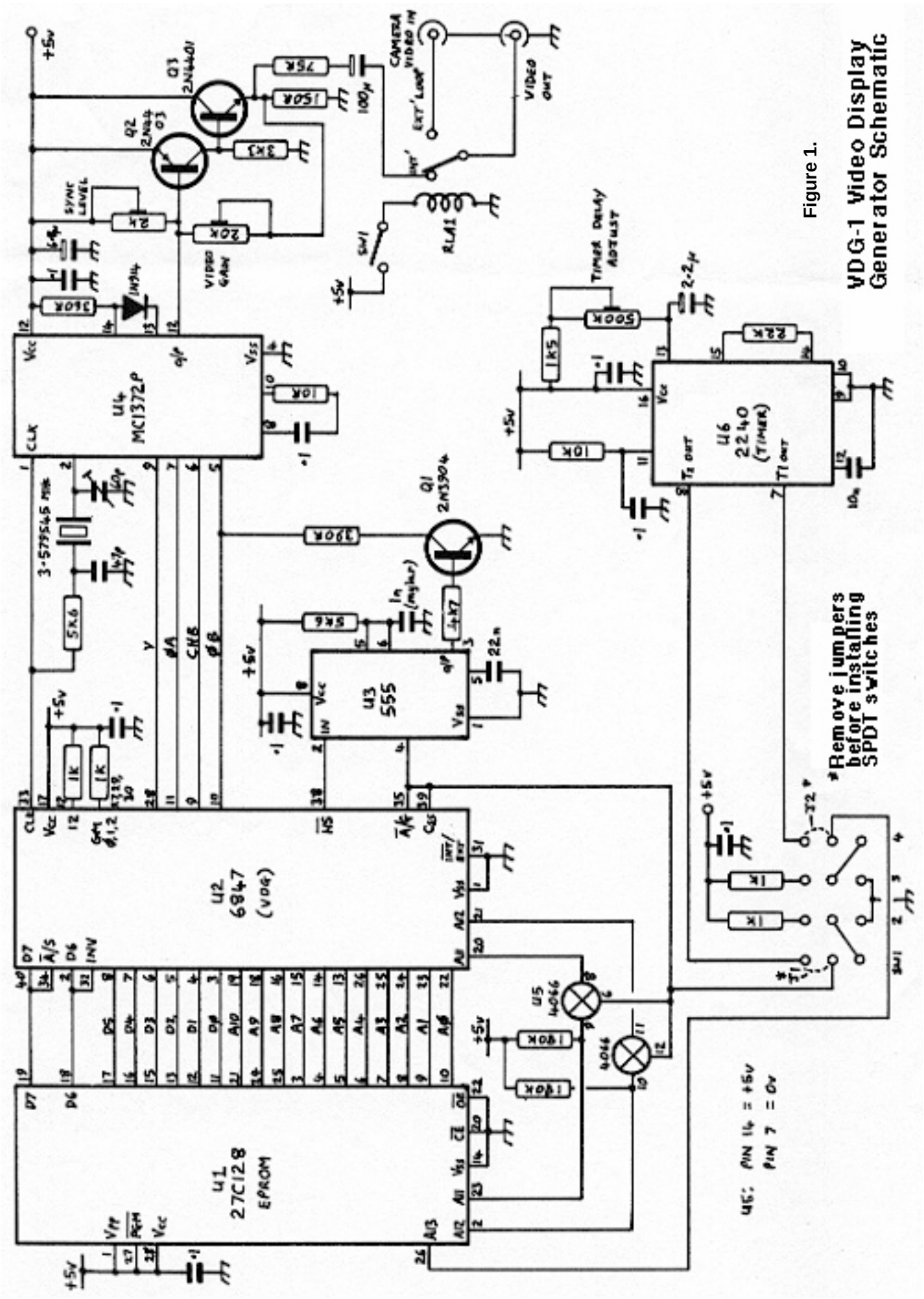
VDG-1 Video Display Generator Schematic
*Remove jumpers before installing SPDT switches
U1 27C128 EPROM
U2 6847 (VDG)
U3 555
U4 MC1372P
U5 4066
U6 2240 (TIMER)
Q1 2N3904
Q2 2N4403
Q3 2N4401
RLA1
SW1
CAMERA VIDEO IN
EXT' LOOP
VIDEO OUT
SYNC LEVEL
VIDEO GAIN
TIMER DELAY ADJUST
3·579545 MHz
+5V
U6: PIN 14 = +5V
PIN 7 = 0V

Figure 1.

ADDITIONAL INFORMATION

If you are using a quick release E-PROM socket remember to turn off the power before changing the memory device. (This also applies even if you are using a standard socket). Ensure that the locator spot on the E-PROM is aligned correctly with the one on the socket. The E-PROM is a static-sensitive device, and as such should be stored on static-resistant foam or in a plastic storage tube when not in circuit.

For those who wish to experiment with the colour-burst circuitry the 5.6k resistor adjacent to the 555 timer can be replaced with a 10k potentiometer. This will allow the number of cycles of burst in the high-resolution mode to be varied. Also, the 10-ohm resistor adjacent to the MC1372P IC can be replaced with a 1k potentiometer in order to vary the amplitude of the burst signal. The locations of both resistor changes are shown on the inset in Fig.5.

Horizontal sync pulses can be found on pin-38 of the VDG, and vertical sync on pin-37. The 3.579545MHz clock signal can be found on pin-1 of the MC1327P IC.

For further information, or to order the unit please write to:

Bill Brown, WB8ELK, 107 Woodlawn Dr., Madison AL 35758
http://www.elktronics.com, wb8elk@aol.com, (256)772-6000

For a nominal fee Bill is also happy to layout your graphic screens from your designs and program the E-Proms with the data.